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EXAMINER	
HUYNH, KIM T	

ART UNIT	PAPER NUMBER
2189	9

DATE MAILED: 12/09/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/490,132	MOYER, WILLIAM C.	
	Examiner	Art Unit	
	Kim T. Huynh	2189	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE ____ MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 September 2003*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *14-16 and 22* is/are allowed.

6)☒ Claim(s) *1-5,8-13 and 19-21* is/are rejected.

7)☒ Claim(s) *6 and 17* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *1/24/00* is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

2. The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

3. Claims 1, 3-5 and 8, 19-21 are rejected under 35 U.S.C. 102(e) as being anticipated by Arndt et al. (US Patent 5,701,495)

As per claims 1, 8, Arndt discloses a method for implementing interrupts in a data processing system, comprising the steps of:

- providing a first storage device (fig.5, 56) having a plurality of inputs , each of the plurality of inputs (interrupt signals) being coupled by a respective physical conductor to one of a plurality of hardware-generated interrupt sources (col.7, lines

6-13) which selectively generate hardware interrupts and selectively storing the hardware interrupts, the first storage device providing one or more hardware-generated interrupt signals. *[(note, storage queue (56) comprises plurality of hardware interrupts which generated by I/O controller (fig.2, 34) , (col.4, lines 25-52), (col.8, lines 56-67), wherein interrupt signals associated with a particular processor implies interrupt signals associated with physical conductor*]

- providing a second storage device (fig.5, 57) having one or more inputs, each of the one or more inputs (means interrupt signals) receiving and storing a predetermined one of a plurality of software-generated interrupt signals, at least some of the predetermined plurality of software-generated interrupt signals indicating an interrupt from a different source or of a different type than the hardware interrupts, the second storage device providing one or more software-generated interrupt signals. [*(col.9, lines 1-5), (col.8, lines 6-12), wherein queue 57 comprises plurality of software and hardware interrupts signals which can be specified by value of external interrupt source register), (col.18, lines 20-27), (col.2, lines 19-43)*
- coupling logic circuitry (fig.5, 55) to the first storage device and the second storage device for receiving the one or more hardware-generated interrupt signals and the one or more software-generated signals, the logic circuitry providing an

interrupt request signal which will cause an interrupt to occur in the data processing system. *[(fig.5, 55 queues wherein receiving and selecting plurality of interrupts types from the hardware and software queues in 56 and 57, (col.8, lines 62-65), (col.9, lines 1-6)]*

- a plurality of hardware interrupt sources *[(fig.5, 56); (col.7, lines 7-21)]*
- executing software with the data processing system to generate a predetermined software-generated interrupt signal which emulates a predetermined one of the hardware-generated interrupt sources but with a priority which differs from the predetermined one of the hardware-generated interrupt sources, thereby dynamically changing prioritization of servicing of interrupts in the data processing system; *[(col.10, lines 1-23), (col.9, lines 55-67), (col.12, lines 56-65), note, an assigned value interrupt is signaled to processor by the hardware via interrupt signal into the processor hardware, then the software receive and read and store this value once this interrupt has been presented this will signals hardware that software will start processing this implies emulation ,furthermore, software sets and removes priority which implies changing prioritization of servicing.)]*
- assigning an interrupt prioritization level to storage locations of the first storage device and the second storage device. (*fig.5, 56, for hardware interrupts*) and the second storage device *(fig.5, 57 for software interrupts) (24-31 bits field which specifies what priority should be assigned to the incoming interrupt, see the XIVR*

Register for description) col.11, table 2, (col.6, lines 64-67), (col.7, lines 1-5)), Examiner further cited (col.8, line 56-col.9, line 12) for clarification, Since the step of selecting the highest priority by routing layer 55 between the storages interrupts queues 56 and 57, it is inherent the layer 55 is assigning an interrupt prioritization level between the two)

As per claims 3 and 19, Arndt discloses a method further comprising the step of assigning a portion of the plurality of software-generated interrupt signals stored in the second storage device to represent interrupts from some interrupt sources generating hardware interrupt and having a corresponding interrupt prioritization level *[(col.4, lines 25-32), note from fig.5, 55 step of selecting the priority between hardware and software interrupts from fig.2, 42&43 storage queues comprise list of prioritized list of events associated with a logical server)]*

As per claims 4 and 20, Arndt discloses a method further comprising the step of assigning a portion of the plurality of software-generated interrupt signals stored in the second storage device to represent interrupts from same interrupt sources generating hardware interrupts and having an interrupt prioritization level which differs from the interrupt prioritization level of the plurality of hardware-generated interrupt sources coupled to the first storage device *[(col.4, lines 1-67), note from fig.5,55 step of selecting priority between hardware and software interrupts from fig.2, 42&43 storage queues comprise list of prioritized list of events; events are from external interrupts from IOC and inter-processor interrupts)]*

As per claims 5 and 21, Arndt discloses method further comprising the step of changing interrupt servicing from servicing a hardware-generated interrupt and switching to servicing a software-generated interrupt of

higher prioritization before completion of servicing of the hardware-generated interrupt occurs. *[(col.10, lines 12-23) (note, software remove and sets what interrupt servicing routing to revoke, (col.6, lines 45-63), changing operation priority implies changing interrupts services)]*

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 2, 9, 12, are rejected under 35 U.S.C. 103(a) as being unpatentable over Arndt et al (US Patent 5,701,495) in view of Simpson et al. (US Patent 6,185,629)

As per claim 2, Arnedt discloses all the limitations as above except the limitation that determining priority between two interrupts, a first interrupt being hardware-generated and a second interrupt being software-generated, when the two interrupts have a same prioritization level by choosing to service one of the hardware-generated first interrupt or the software-generated second interrupt. However, Simpson discloses determining priority for multiple requests from different processors of the same priority, it will form a round robin between them round robin will always be passed to the next processor with a pending request in the

chain, this prevents requests of equal priority from other processors need to be serviced. (col.25, lines 17-27)

It would have been obvious one having ordinary skills in the art at the time the invention was made to incorporate Simpson's teaching into Arndt's method to include the round robin for determining the priority between the same prioritization level between software and hardware so as to be advanced avoiding interrupts suspended due to time-out fault or error. (col.72, lines 55-67)

As per claim 9 Arndt discloses:

- providing a first storage device (fig.5, 56) having a plurality of inputs , each of the plurality of inputs (interrupt signals) being coupled by a respective physical conductor to one of a plurality of hardware-generated interrupt sources (col.7, lines 6-13) which selectively generate hardware interrupts and selectively storing the hardware interrupts, the first storage device providing one or more hardware-generated interrupt signals. *[(note, storage queue (56) comprises plurality of hardware interrupts which generated by I/O controller (fig.2, 34) , (col.4, lines 25-52), (col.8, lines 56-67), wherein interrupt signals associated with a particular processor implies interrupt signals associated with physical conductor*]
- providing a second storage device (fig.5, 57) having one or more inputs, each of the one or more inputs (means interrupt

signals) receiving and storing a predetermined one of a plurality of software-generated interrupt signals, at least some of the predetermined plurality of software-generated interrupt signals indicating an interrupt from a different source or of a different type than the hardware interrupts, the second storage device providing one or more software-generated interrupt signals. [*(col.9, lines 1-5), (col.8, lines 6-12), wherein queue 57 comprises plurality of software and hardware interrupts signals which can be specified by value of external interrupt source register), (col.18, lines 20-27), (col.2, lines 19-43)*

- coupling logic circuitry (fig.5, 55) to the first storage device and the second storage device for receiving the one or more hardware-generated interrupt signals and the one or more software-generated signals, the logic circuitry providing an interrupt request signal which will cause an interrupt to occur in the data processing system. *[(fig.5, 55 queues wherein receiving and selecting plurality of interrupts types from the hardware and software queues in 56 and 57, (col.8, lines 62-65), (col.9, lines 1-6)]*
- a plurality of hardware interrupt sources *[(fig.5, 56); (col.7, lines 7-21)]*
- executing software with the data processing system to generate a predetermined software-generated interrupt signal which emulates a predetermined one of the hardware-generated interrupt sources but with a priority which differs

from the predetermined one of the hardware-generated interrupt sources, thereby dynamically changing prioritization of servicing of interrupts in the data processing system;

[(col.10, lines 1-23), (col.9, lines 55-67), (col.12, lines 56-65), note, an assigned value interrupt is signaled to processor by the hardware via interrupt signal into the processor hardware, then the software receive and read and store this value once this interrupt has been presented this will signals hardware that software will start processing this implies emulation ,furthermore, software sets and removes priority which implies changing prioritization of servicing.)]

Arnedt discloses all the limitations as above except the limitation that determining priority between two interrupts, a first interrupt being hardware-generated and a second interrupt being software-generated, when the two interrupts have a same prioritization level by choosing to service one of the hardware-generated first interrupt or the software-generated second interrupt. However, Simpson discloses determining priority for multiple requests from different processors of the same priority, it will form a round robin between them round robin will always be passed to the next processor with a pending request in the chain, this prevents requests of equal priority from other processors need to be serviced. (col.25, lines 17-27)

It would have been obvious one having ordinary skills in the art at the time the invention was made to incorporate Simpson's teaching into Arndt's method to include the round robin for determining the priority

between the same prioritization level between software and hardware so as to be advanced avoiding interrupts suspended due to time-out fault or error. (col.72, lines 55-67)

As per claim 12, Arndt discloses a mask register coupled to the hardware interrupt storage device and the software interrupt storage device for selectively preventing hardware-generated interrupt signals and software-generated interrupt signals from propagating to the logic circuitry. *(col.12, lines 10-31)*

As per claim 13, Arndt discloses the hardware interrupt storage device and the software interrupt storage device are each implemented as latch circuits *[(fig.1, 34) note, interrupt signals control and configure by controller (fig.2, 34), (col.4, lines 17-24)]*

6. Claims 10-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Arndt et al. (US Patent 5,701,495) in view of Simpson et al. (US Patent 6,185,629) and further in view of Donovan (US Patent 5,987,601)

The modified system of Arndt further discloses:

- the hardware interrupt storage device and the software interrupt storage device have an assigned interrupt prioritization level to specific storage locations, *(col.4, lines 53-61)*
- assignment of the interrupt prioritization level of interrupt sources associated with the software-generated interrupt signals being variable by software control.(*col.10, lines 19-22,*

col.9, lines 16-25),note the software removes and sets priority in the queue)

- a software-generated interrupt signal of higher priority than a currently executing hardware-generated interrupt signal is provided to the logic circuitry prior to completion of an associated hardware interrupt servicing, and the data processing system suspends processing of the hardware interrupt servicing to process an associated software interrupt servicing. *(col.6, lines 45-63)*

Arndt discloses all the limitation as above except the limitation that the interrupt prioritization level of the hardware interrupt sources being permanently assigned. However, Donavan discloses the major interrupt sources is assigned a fixed hardware task number. *(col.5, lines 57-62)*

It would have been obvious to one having ordinary skills in the art at the time the invention was made to incorporate Donavan's teaching into Arndt's method to have the hardware interrupt source being permanently assigned so as to limiting the number of tasks change in the system. *(col.2, lines 16-22)*

CLAIMS OBJECTION

7. Claims 6, 17 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

As per claims 6 and 17, Prior art does not teach or suggest the step of changing prioritization level of a predetermined hardware-generated interrupt by providing a software-generated interrupt which represents a corresponding hardware-generated interrupt source for the predetermined hardware-generated interrupt but with a different prioritization level than the predetermined hardware-generated interrupt.

Allowable Subject Matter

8. Claims 14-16, 22 are allowable.

The following is an examiner's statement of reasons for allowance:

As per claims 14-16, 22, Applicant's claimed invention is deemed allowable over the prior art of record as the prior art fails to teach or suggest the step of changing prioritization level of a predetermined hardware-generated interrupt by providing a software-generated interrupt which represents a corresponding hardware-generated interrupt source for the predetermined hardware-generated interrupt but with a different prioritization level than the predetermined hardware-generated interrupt in combination with other limitations as recited in independent and further in view of the specification and applicant's arguments and references cited by Examiner.

Response to Arguments

9. Applicant's arguments filed on 9/26/03 have been considered but are not persuasive.

a. Applicant argues that Arndt does not disclose assigning an interrupt prioritization level to storage locations of the first storage device and the second

storage device and the second storage device. Examiner respectively disagrees. As Arndt notes at (*fig.5, 56, for hardware interrupts*) for the first storage device and the second storage device *(fig.5, 57 for software interrupts), Examiner further cited (col.8, line 56-col.9, line 12) for clarification, Since the step of selecting the highest priority by routing layer 55 between the storages interrupts queues 56 and 57, it is inherently implying the layer 55 is assigning an interrupt prioritization level between the two)*

b. Applicant argues that Simpson teaches the using a round robin scheme to determine priority between multiple requests received with the same priority. However, there is no teaching or suggestion of using this round robin scheme between hardware-generated interrupts and software-generated interrupts. Round-robin is well known in the art, Examiner further cited Kelsey (Pub. No. 20030037228) for supporting in re Simpson. As Simpson, Kelsey discloses round-robin between selecting thread (hardware or software interrupt) [0081]

Conclusion

10. THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will

the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kim Huynh whose telephone number is (703)305-5384 or via e-mail addressed to [kim.huynh3@uspto.gov]. The examiner can normally be reached on M-F 8:30AM-6:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on (703) 305-4815 or via e-mail addressed to [mark.rinehart@uspto.gov]. The fax phone numbers for the organization where this application or proceeding is assigned are (703)872-9306 for regular communications and After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)306-5631.

Kim Huynh

Dec. 1, 2003

Khanh Dang
Primary Examiner